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(71) Applicant(s)
Winbond Electronics Corp.

(Incorporated in Taiwan)

No 2 R&D Rd VI, Science Based Industrial Park, Hsinchu, Taiwan

(72) Inventor(s)
Tsuei-Chi Yeh

(74) Agent and/or Address for Service
Gill Jennings & Every
Broadgate House, 7 Eldon Street, LONDON, EC2M 7LH, United Kingdom

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(56) Documents Cited
GB 2206431 A GB 2205186 A GB 1543602 A
US 4795893 A US 4105156 A

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(54) **Intergrated circuit**

(57) An integrated circuit (1) destroys itself by a voltage signal generated therein when a predetermined condition is met. The integrated circuit comprises a transistor (11) and a fuse-type switch device (13). The transistor (11) has a control terminal (110) coupled to a first reference voltage (V1) initially to enable the integrated circuit. The fuse-type switch device (13), in response to a voltage signal, couples the control terminal to a second reference (V2) thereby disabling the function of the integrated circuit permanently.

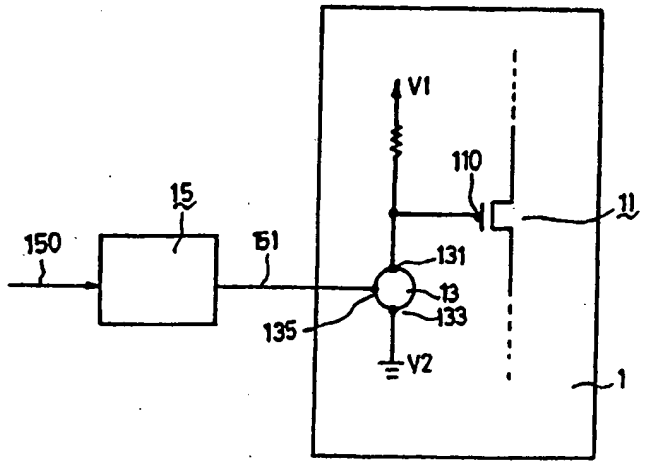

FIG.1

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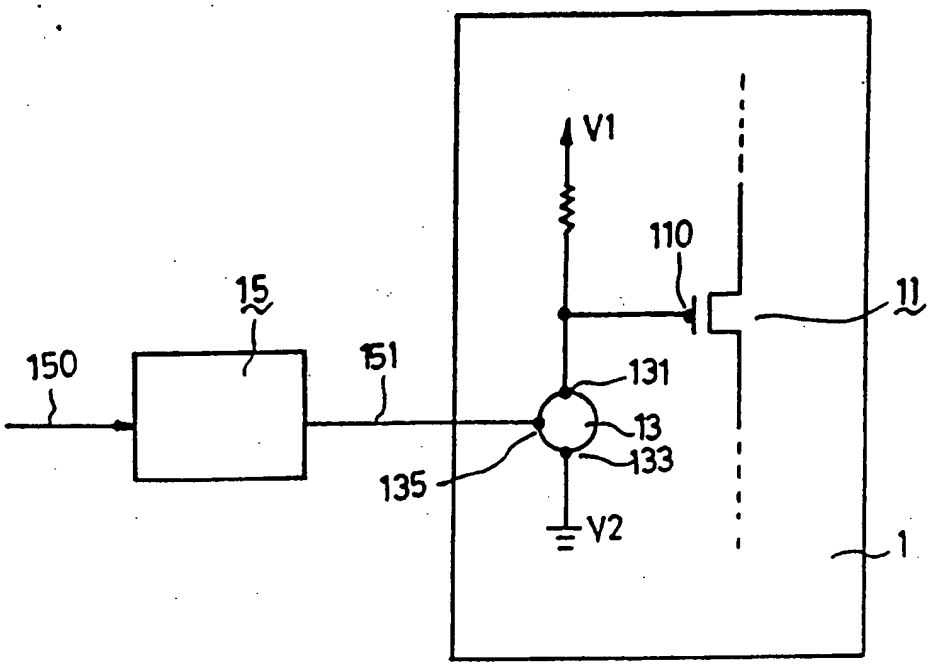

FIG.1

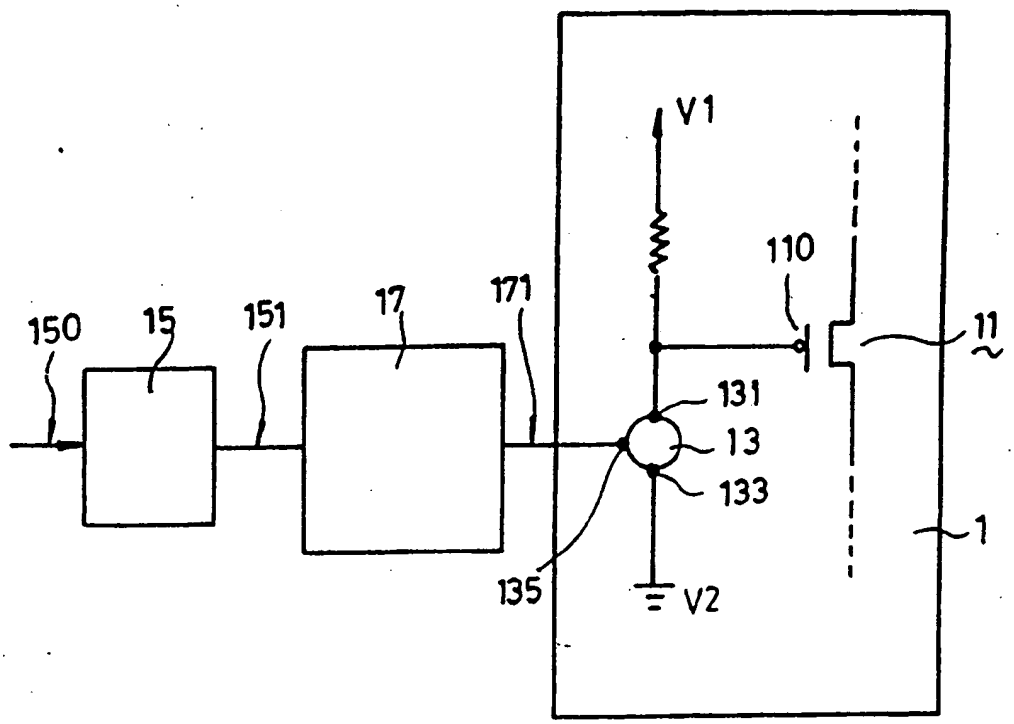
V1
110
11
150
15
151
17
171
131
13
133
1
135
V2

FIG.2

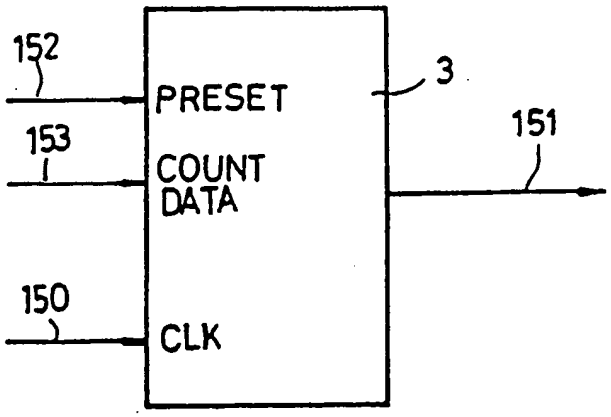
152
PRESET
3
151
153
COUNT
DATA
150
CLK

FIG.3

INTEGRATED CIRCUIT

The invention relates to an integrated circuit.

Typically, an integrated circuit is designed and manufactured to meet the specification of the integrated circuit. In most design specifications, the life time of the integrated circuit or the number of times the integrated circuit is powered up is expected to be as long or as large as possible, and has no upper limit. The specification of the conventional integrated circuit products all belong to the kind just recited.

However, in few special applications, the producer of the integrated circuit or the downstream system maker prefers to cease the life of the integrated circuit when a predetermined condition occurs or limit the number of times the integrated circuit is powered up. For

instance, in the area of integrated circuit relating to the computer game, it is occasionally expected the computer game cannot be played any more when a predetermined condition is occurred. The predetermined condition may include, among others, a predetermined number of times the integrated circuit is powered up, an execution of comparison of a particular address, or a predetermined accumulated time the computer game is run, etc. To name another, an electric key system may be also a good example of field of use of this special specification. When a holder of an electronic key, or IC card, does not respond to a security system correctly within a predetermined number of input occasions of the assigned password, the integrated circuit within the IC card will destroy itself in order to prevent further use of the card.

In order to meet the need of this special application, the present invention provides an integrated circuit which destroys the function of the integrated circuit when a predetermined condition is met.

In accordance with the present invention, an integrated circuit comprises a transistor having a control terminal coupled to a first reference voltage initially to enable said integrated circuit; and a fuse-type switch means for coupling said control terminal to a second reference voltage in response to a control signal in order to disable the function of said integrated circuit permanently.

The self-destructive integrated circuit provided in the invention comprises a transistor and a fuse-type switch device. The transistor has a control terminal coupled to a first reference voltage initially to enable the integrated circuit. The fuse-type switch device, in response to a control, e.g. voltage, signal, couples the control terminal to a second reference voltage in order to disable the function of the integrated circuit permanently. The control signal is generated when a predetermined condition occurs.

The invention will be further understood by reference to the following detailed description of the invention, together with the appended drawings, in which:-

FIG. 1 discloses a first preferred embodiment of the invention;

FIG. 2 discloses a second preferred embodiment of the invention; and,

FIG. 3 discloses a preferred embodiment of the destructive qualifying device of the invention.

As shown in FIG. 1, the integrated circuit 1 of the invention includes a transistor 11 and a fuse-type switch device 13. The transistor 11 has a control terminal 110 coupled to a first reference voltage V1 initially to enable the integrated circuit 1. In other words, as the control terminal 110 is coupled to the first reference voltage V1, the integrated circuit 1 functions as designed.

The fuse-type switch device 13 couples the control terminal 110 to a second reference voltage V2 when a voltage signal 151 is asserted thereto from a destruction-qualifying device 15. As a result, the integrated circuit 1 is disabled or malfunctioned permanently to the user of the integrated circuit 1.

The transistor 11 chosen may be any power switch or logic gate in the integrated circuit 1, as long as its disability will enforce the integrated circuit 1 to malfunction or not to function.

Depending on the detailed design of the integrated circuit 1, the transistor 11 may be a

MOS field-effect transistor, a bipolar transistor or a Junction field-effect transistor.

Depending on the type of the transistor 11 selected in the integrated circuit 1, the control terminal 110 may be the gate, drain or source terminal of a MOS or Junction field-effect transistor, or may be the base, emitter or collector terminal of a bipolar transistor.

The fuse-type switch device 13 has a first terminal 131, a second terminal 133 and a signal input terminal 135. The first terminal 131 is coupled to the control terminal 110 and the second terminal 133 is coupled to the second reference voltage V2. The first terminal 131 has relation of a first kind with the second terminal 133 initially. The signal input terminal 135 is adapted to receive the voltage signal 151 such that the first terminal 131 has relation of a second kind with the second terminal 133 as the voltage signal 151 is asserted. The relation of the first kind is opposite to the relation of the second kind. The first, or the second, kind relation includes electrically-connected relation and electrically-disconnected relation, all depending on the type of the transistor 11, the control terminal 110 , and the first and second reference voltage V1, V2 selected.

As the first reference voltage V1 is selected to be a reference high, the second reference voltage V2 should be selected to be a reference low. On the contrary, as the first reference voltage V1 is selected to be a reference low, the second reference voltage V2 should be selected to be a reference high.

The fuse-type switch device 13 may be embodied through the form of a silicon fuse, a non-volatile memory cell, a silicon anti-fuse, or a polysilicon-fuse. A one-time-programmable read only memory(OTPROM) cell, an electrical erasable programmable read only memory (EEPROM) cell, or a ferro-electric random access memory (FERAM) cell is a

preferred selection among the different types of the non-volatile memory cell. An erasable programmable read only memory (EPROM) is a straightforward choice among different types of OTPROM.

The destructive qualifying device 15 generates the voltage signal 151, responsive to an event signal 150 which is generated by the circuits of a system incorporating the integrated circuit 1. The destructive qualifying device 15 may be a circuit inside or outside the integrated circuit 1.

A preferred embodiment of the destructive qualifying device 15 is a counter/timer 3 shown in FIG. 3. The counter/timer 3 shown is a non-volatile presettable one, which has a preset terminal receiving a preset signal 152, count data terminal receiving a count data signal 153 and a clock terminal receiving the event signal 150. The event signal 150 may be a power-up signal, a particular address comparison signal or any other type of signal that can be used to count down the counter/timer 3. The predetermined count data 153 is fed to the count data terminal as the preset terminal is pulled active in order to preset the counter/timer 3 at the final stage of the manufacture of the integrated circuit 1.

As recited above, there are many different selections for the fuse-type switch device 13. However, for different types of fuse-type switch device 13, there corresponds to different minimum electrical voltage required to change the state of the fuse-type switch device 13.

Therefore, a second preferred embodiment of the invention , as shown in FIG. 2, may be recommended for some types of the fuse-type switch device 13.

All elements of FIG. 2, except a voltage charge pump 17, are the same as those disclosed in FIG. 1, therefore, the function and the operation thereof may be referred to the

corresponding recitations above, and will not be further recited hereinafter.

As shown in FIG. 2, the voltage charge pump 17 is triggered by a qualification signal 151 from the destructive qualifying device 15 to generate a voltage signal 171 of a much higher voltage which is required to change the state of some types of the fuse-type switch device 13.

Same as the destructive qualifying device 15, the voltage charge pump 17 may be a circuit inside or outside the integrated circuit 1.

CLAIMS

1. A circuit comprising:

a transistor having a control terminal coupled to a first reference voltage initially to enable said integrated circuit; and

a fuse-type switch means for coupling said control terminal to a second reference voltage in response to a control signal in order to disable the function of said integrated circuit permanently.

2. The integrated circuit as recited in claim 1, wherein said transistor is a MOS field-effect transistor.

3. The integrated circuit as recited in claim 1, wherein said transistor is a bipolar transistor.

4. The integrated circuit as recited in claim 1, wherein said transistor is a junction field-effect transistor.

5. The integrated circuit as recited in claim 2, wherein said control terminal is a gate terminal of said MOS field-effect transistor.

6. The integrated circuit as recited in claim 3, wherein said control terminal is a base terminal of said bipolar transistor.

7. The integrated circuit as recited in claim 4, wherein said control terminal is a gate terminal of said junction field-effect transistor.

8. The integrated circuit as recited in any of the preceding claims, wherein the fuse-type switch means has a first terminal, a second terminal and a signal input terminal, said first terminal being coupled to said control terminal and said second terminal being coupled to said second reference voltage, the first terminal having a relation of a first kind with the second terminal initially, said signal input terminal being adapted to receive said control signal such that said first terminal has relation of a second kind with said second terminal as said control signal is asserted.

9. The integrated circuit according to any of the preceding claims, wherein said first reference voltage is a reference high and said second reference voltage is a reference low.

10. The integrated circuit according to any of claims 1 to 8, wherein said first reference voltage is a reference low and said second reference voltage is a reference high.

11. The integrated circuit according to any of the preceding claims, wherein said fuse-type switch means is in the form of a silicon-fuse.

12. The integrated circuit according to any of claims 1 to 10, wherein said fuse-type switch means is in the form of a non-volatile memory cell.

13. The integrated circuit according to any of claims 1 to 10, wherein said fuse-type switch means is in the form of an anti-fuse.

14. The integrated circuit according to any of claims 1 to 10, wherein said fuse-type switch means is in the form of a polysilicon-fuse.

15. The integrated circuit as recited in claim 12, wherein said non-volatile memory cell is a ferro-electric random access memory (FERAM) cell.

16. The integrated circuit as recited in claim 12, wherein said non-volatile memory cell is a one-time-programmable read only memory (OTPROM) cell.

17. The integrated circuit as recited in claim 16, wherein said OTPROM is an erasable programmable read only memory (EPROM) cell.

18. The integrated circuit as recited in claim 12, wherein said non-volatile memory cell is an electrical erasable programmable read only memory (EEPROM) cell.

19. The integrated circuit according to any of the preceding claims, further comprising:

a destruction qualifying circuit for generating said control signal in response to an event signal.

20. The integrated circuit according to claim 19, further comprising:

a voltage charge pump for generating said voltage signal in response to said qualification signal.

21. The integrated circuit as recited in claim 19 or claim 20, wherein said destructive qualifying circuit is a counter/timer having a clock input receiving said event signal.

22. The integrated circuit as recited in claim 21, wherein said event signal is a power-up signal.

23. The integrated circuit as recited in claim 21, wherein said event signal is an address comparison signal.

24. The integrated circuit according to at least claim 8, wherein the first kind of relation is an electrically-connected relation and the second kind of relation is an electrically-disconnected relation.

25. The integrated circuit according to claim 8 or any of claims 9 to 23 when dependent on claim 8, wherein the first kind of relation is an electrically-disconnected relation and the second kind of relation is an electrically-connected relation.

26. An integrated circuit according to any of the preceding claims, wherein the control signal is a voltage signal.

27. An integrated circuit substantially as hereinbefore described with reference to any of the examples shown in the accompanying drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 (The Search report)	Application number GB 9406263.5
Relevant Technical Fields (i) UK Cl (Ed.M) G4H (HTG), HIK (KGPX) (ii) Int Cl (Ed.5) G07C, G07F	Search Examiner M J DAVIS
	Date of completion of Search 17 MAY 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii)	Documents considered relevant following a search in respect of Claims :- 1 TO 27

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Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2206431 A	(MOTOROLA) whole document	1-27
X	GB 2205186 A	(MOTOROLA) whole document	1-27
X	GB 1543602	(SOCIETE...) eg page 8 lines 52 to page 9 line 41	1-27
X	US 4795893	(UGON) whole document	1-27
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